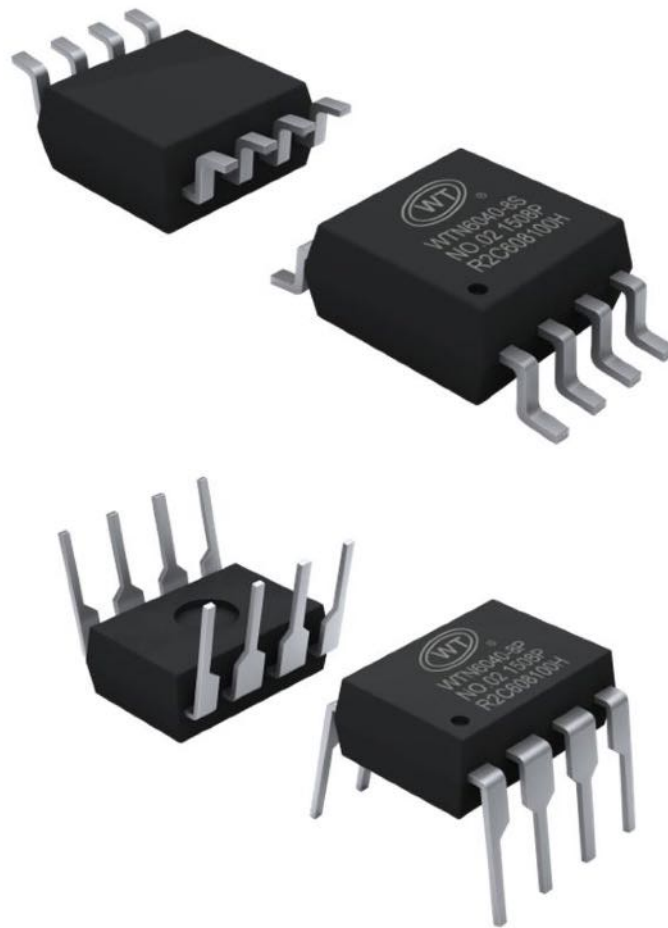


WTN6 Series of Voice Chip

Version : V1.06



Note :

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1. Overview

The WTN6 series are multifunctional, low-power, high-performance CMOS voice chips. There are three types of chips, WTN6040, WTN6096, and WTN6170 (voice lengths are 40s, 96s, 170s, respectively). WTN6040, WTN6096, and WTN6170 have been put on the market. The audio sampling rate is currently up to 32kHz, 16-level volume control, and two audio output modes: PWM output and DAC output. Accurate +/-1% internal oscillation, no need to add external oscillation, with ultra-low power standby.

2. Functions

- Working voltage: 2.4V~5.2V.
- In standby mode, quiescent current less than 5uA (After the voice playback is completed, the DATA/CLK signal line can stay at a stable level for about 2 seconds to sleep)
- Accurate +/-1% internal oscillation, with low voltage reset (LVR=1.8V) watchdog timing
- PWM audio output, able to drive 8Ω/0.5W speaker and buzzer directly; DAC audio output, able to have external amplifier.
- Built in watchdog.
- With serial port control mode: count pulse, button, one-line serial port, two-line serial port (up to 224 voices can be loaded, detailed explanation will be provided later)
- Support output function in BUSY state(The BUSY pin of the standard program defaults to high level, and it is low level during voice playback. In addition, in the serial port control mode, only when the voice chip receives the correct voice address sequence BUSY pin will there be a level change)

Selection Attention:

- 1. The control mode and output mode of the chip have been set when the program is programmed, and cannot be changed again. When ordering the chip, it is necessary to explain the application requirements to the salesperson.**
- 2. Because WTN6 needs a certain initialization time (about 100MS) to power on, and it cannot respond to commands during initialization, it needs to complete initialization to receive control normally.**

3.WTN6 chip two-line serial port control DAC output DEMO board playback effect plus communication timing demo video:https://v.youku.com/v_show/id_XNDcwMzM5MDMwOA==.html?spm=a2h0c.8166622.PhoneSokuUgc_1.dtitle

4.WTN6 chip one-line serial port control PWM output DEMO board playback effect plus communication timing demo video:https://v.youku.com/v_show/id_XNDcwMzM4NzI1Ng==.html?spm=a2h0c.8166622.PhoneSokuUgc_1.dtitle

3. Pin Description



3.1. Pin Distribution Diagram

Pin Name	No.	ATTR.	Description
PA2	1	I/O	Output the busy signal
PA1	2	I/O	Two-line serial port clock signal input terminal/ one-line serial port data signal input terminal/Count pulse data signal input terminal
PA0	3	I/O	Two-line serial port data signal input terminal/reset pin
PA3	4	I/O	Not use
PWM-	5	out	PWM output pin
VDD	6	Power	Positive electrode
PWM+/DAC	7	I/O	PWM, DAC output pin
GND	8	Power	Negative electrode

4. Limited Parameters

Mark	Range	Unit
VDD~GND supply voltage	-0.5~+5.2	V
Vin input voltage	GND-0.3< Vin <VDD+0.3	V
Vout output voltage	GND < 0.3V ~ VDD+0.3	V
Top storage temperature	-20~ +75 (Use with caution in industrial special occasions)	°C

Remarks: As a result of the samples tested in the laboratory, the chip can work normally at -20°C~+75°C.

5. DC Characteristics

Mark	Parameters	Min.	Typical value	Max.	Unit	Condition
VDD	Working voltage	2.4	3.0	5.2	V	1MHz or 2MHz
I _{sb}	Standby current, VDD=3V/4.5V			3.1	uA	No load
I _{op}	Working current	VDD=3V	3		mA	
		VDD=4.5V	3.7		mA	
I _{IK}	input leakage current		0.1		uA	
I _{oh}	Output drive current		10		mA	VDD=3V, Voh=1.0V
			22		mA	VDD=4.5V, Voh=2.2V
I _{ol}	Output reverse current		20		mA	VDD=3V, Voh=2.0V
			40		mA	VDD=4.5V, Voh=2.5V
I _{oh}	PWM1 output current		60		mA	VDD=3V, Load=8 ohms
			100		mA	VDD=4.5V, Load=8 ohms
I _{oh}	PWM2 output current			70	mA	VDD=3V, Load=8 ohms
				117	mA	VDD=4.5V, Load=8 ohms
I _{ol} ΔF/F	Voltage fluctuation frequency deviation	VDD=3 V		2		%

		VDD=4.5V		0.5		VDD=4.5V, Load=8 ohms
$\Delta F/F$	Frequency deviation (VDD=3V)	-5		5	%	$\frac{F_{osc(3.0v)} - F_{osc(2.4v)}}{F_{osc(3v)}}$
F_{osc}	oscillation frequency	1.80	2	2.05	Mhz	$\frac{F_{osc(4.5v)} - F_{osc(3.0v)}}{F_{osc(4.5v)}}$
						$\frac{F_{max(3.0v)} - F_{min(3.0v)}}{F_{max(3.0v)}}$ VDD=2.0~5.5V

6. One-line Serial Communication

One-line serial port mode can use MCU to send data to WTN6 series voice chip through DATA line to achieve the purpose of control. It can control voice playback, stop, loop, etc.

6.1. Pin Distribution

Package type	Pins	
	PA1	PA2
SOP8	DATA	BUSY

6.2. One-line audio address corresponding relation

Data(hexadecimal)	Function
00H	The 0th audio play
01H	The 1 st audio play
02H	The 2 nd audio play
.....
DDH	The 221 st audio play
DEH	The 222 nd audio play
DFH	The 223 rd audio play

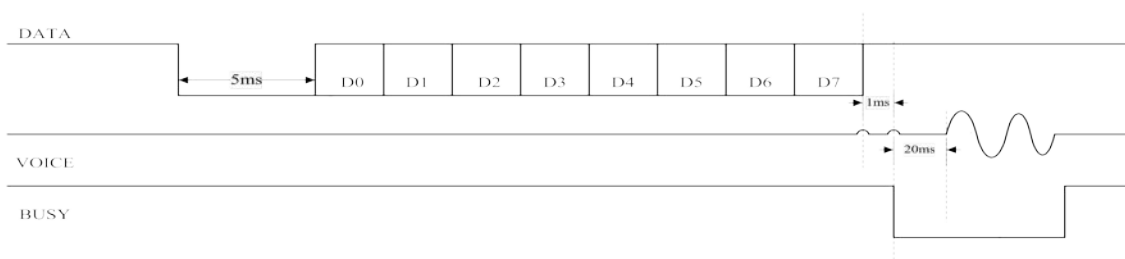
Note: If you want to play the voice of this address, you can automatically play the voice of this address as long as you send the address, and the time interval between the two address commands must be greater than 4ms.

6.3. One-line Audio and Command Code

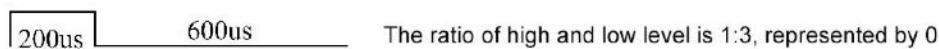
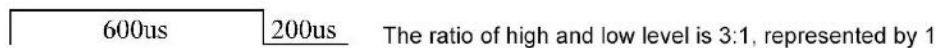
Command code	Function	Description
E0H....EFH	E0 is the minimum volume; EF is the maximum; 16-level volume is adjustable in total.	When the audio play ends, or in standby mode, send this command to adjust volume.
F2H	Repeat to play the current audio	Execute this command to play the current voice in a loop, and it can be sent when the voice is played/stopped. During the execution of the F2 loop command, it can be interrupted by the FE command, ordinary address command, and F3/F8 combined command, and becomes invalid; the playback command must be sent first, and then the loop playback command.
F3H	Concatenated Code play	F3H+audio address A, F3H+audio address B, F3H+audio address C,... When playing address A, the play will be not interrupted even the latter code is received. After finishing playing A, B will be playing, then playing C...need to add 2 ms delay between F3 and the address
F8H	Insert mute	F8H+mute time(10MS as a unit), insert mute after finishing one address play.
FEH	Stop playing the current audio	This command can stop playing the current audio.

Note: Without stopping the playback, if there is no command code F3H or F8H, and only the voice address, the voice that was playing before will be interrupted. The code command must be used in conjunction with the address (for example: F3H+00H+F3H+01H) . F3H and F8H can easily combine different voices, F3H+address+F8H+10H (100ms), up to 10 groups of content can be combined, the first group of commands must be F3+address; you can also judge the BUSY level during voice playback and the end of playback The change of BUSY level completes the combined playback.

6.4. One-line Serial Port Sequence Diagram



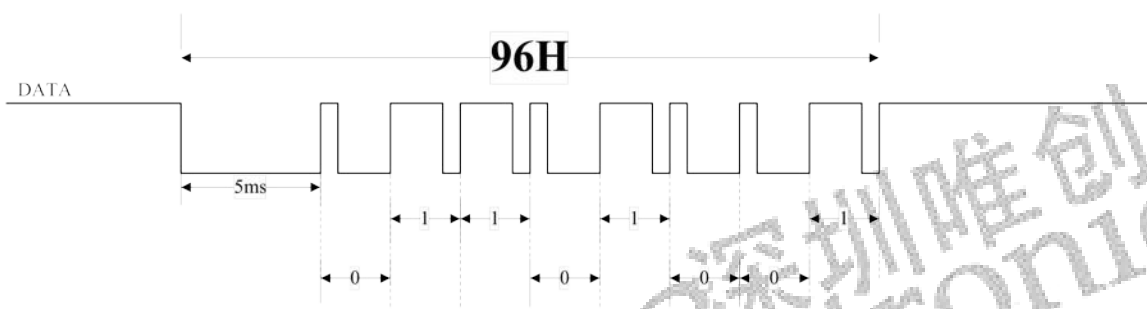
After pulling the data line low for 4-20ms, it is recommended to send 8 bits of data in 5ms. Send the low bit first, then the high bit. Use the ratio of high level to low level to represent the value of each data bit.



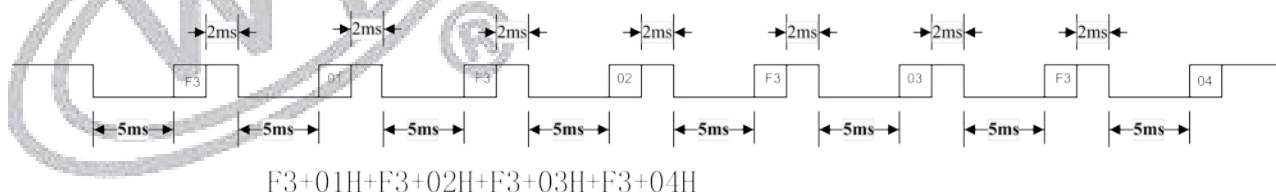
Note: high level in the front, low level at the back.

It is recommended to use 200us: 600us. Value range: 40us:120us ~ 400us:1200us. Pay attention to the use of 3:1 and 1:3 level ratios to ensure stable communication.

If we want to send 96H, then his corresponding sequence diagram is as follows:



If we want the chip to play the voice content of address 01/02/03/04 in turn. That is, the continuous code command play, F3+01+F3+02+F3+03+F3+04. The corresponding timing can be as shown in the following figure:



F3+01H+F3+02H+F3+03H+F3+04H

Note:

1. Because WTN6 needs a certain initialization time (about 100MS) to power on, and it cannot respond to commands during initialization, it is recommended that users use the code-linking function to delay 2ms after sending a group of code-linked addresses before sending the next group of code-linked codes. Address; but the interval between F3 and address is still 2ms;
2. The chip IO port, the default internal 1M pull-down. Therefore, when the customer is doing low-power sleep, the DATA can be pulled down at the end of the voice playback to prevent back flow.

7. Two-line serial port communication

7.1. Pin Distribution

Package type	Pins		
	PA2	PA1	PA0
SOP8/DIP8	Default to BUSY signal output	CLK	DATA

7.2. Audio Address Corresponding Relation

Data(hexadecimal)	Function
00H	The 0th audio play
01H	The 1 st audio play
02H	The 2 nd audio play
.....
DDH	The 221 st audio play
DEH	The 222 nd audio play
DFH	The 223 rd audio play

Note: If you want to play the voice of the address, you can automatically play the voice of the address as long as you send the address. The time interval between the two address commands must be greater than 4ms.

7.3. Audio and Command Code Corresponding Table

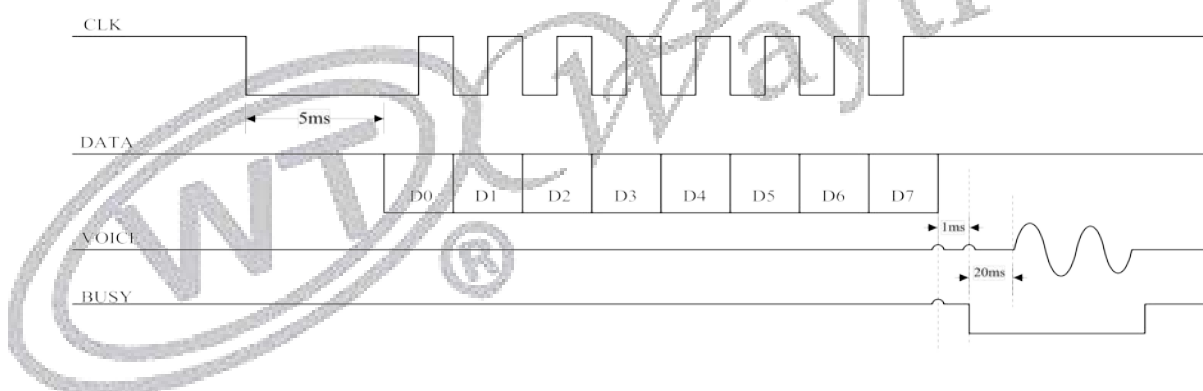
Command code	Function	Description
E0H...EFH	E0 is the minimum volume; EF is the maximum; 16-level volume is adjustable in total.	When the audio play ends, or in standby mode, send this command to adjust volume.
F2H	Repeat to play the current audio	Execute this command to play the current voice in a loop, and it can be sent when the voice is played/stopped. During the execution of the F2 loop command, it can be interrupted by the FE command, ordinary address command, and F3/F8 combined command, and becomes invalid; the playback command must be sent first, and then the loop playback command.

F3H	Concatenated Code play	F3H+audio address A, F3H+audio address B , F3H+audio address C,... When playing address A, the play will be not interrupted even the latter code is received. After finishing playing A, B will be playing, then playing C...,need to add 2 ms delay between F3 and the address.
F8H	Insert mute	F8H+mute time(10MS as a unit), insert mute after finishing one address play.
FEH	Stop playing the current audio	This command can stop playing the current audio.

Note:

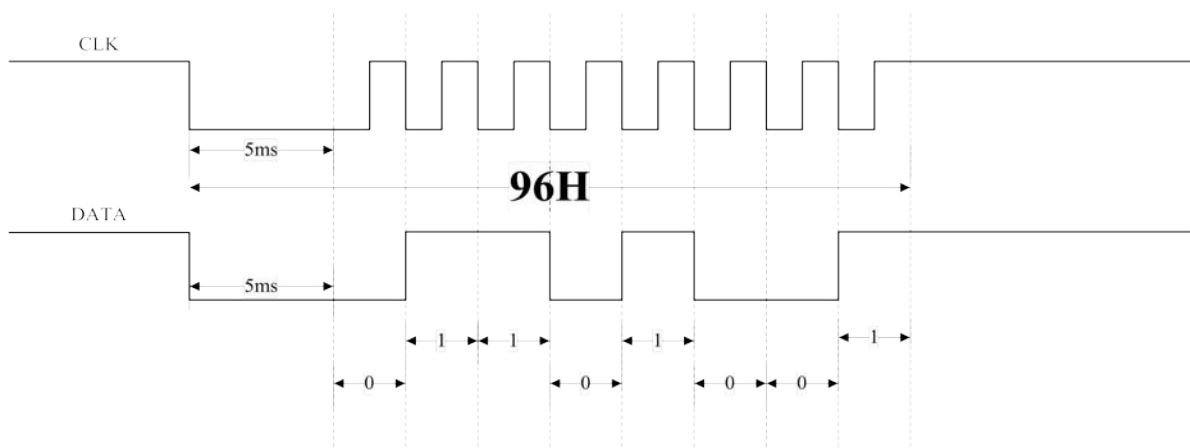
In the case of stopping playback, if there is no command code F3H or F8H and only a voice address, the voice that was playing before will be interrupted, and the code instruction must be used with the address (for example: F3H+00H+F3H+01H). F3H and F8H can easily combine different voices, F3H+address+F8H+10H (100ms), up to 10 groups of content can be combined, the first group of commands must be F3+address; it can also be judged by the BUSY level during voice playback and the end of playback The change of BUSY level completes the combined playback.

7.4. Two-line Serial Port Sequence Diagram



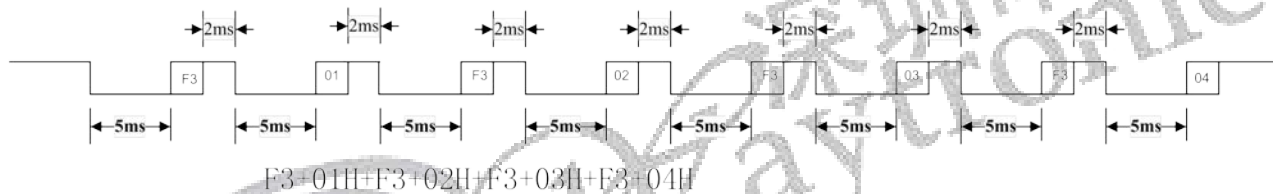
The two-line serial port control mode is controlled by the chip clock CLK and data DATA. Before each byte of data is sent, the clock signal CLK is pulled down 4ms to 20ms. It is recommended to use 5ms to wake up the WTN6 voice chip. Receive data on the rising edge of. The clock cycle is between 100us and 6.4ms, and it is recommended to use 300us for each high and low level duration (that is, the clock cycle for one bit transmission is 600us). When sending data, send the low bit first, then the high bit. 00H~DFH in the data are voice address commands, E0H ~ EFH are volume adjustment commands, F2H is a loop playback command, and FEH is a stop playback command.

If we want to send 96H, then his corresponding sequence diagram is as follows:



If we want the chip to play the voice content of address 01/02/03/04 in turn. That is, the continuous code command play, F3+01+F3+02+F3+03+F3+04.

The corresponding timing can be as shown in the following figure:



Remarks:

1. Because WTN6 needs a certain initialization time (about 100MS) to power on, and it cannot respond to commands during initialization, it is recommended that users use the code-linking function to send a group of coded addresses and then delay 2ms before sending the next group of coded addresses. ; But the interval between F3 and the address is still 2ms;
2. The chip IO port, the default internal 1M pull-down. Therefore, when the customer is doing low-power sleep, the voice playback can pull down CLK and DATA to prevent backflow.

8. Count Pulse Control Mode:

The pulse count control mode is to control the playback of the voice address by sending different pulses on the DATA line. This control mode has simple operation and convenient control, and is often used in occasions where the number of voice segments is not many.

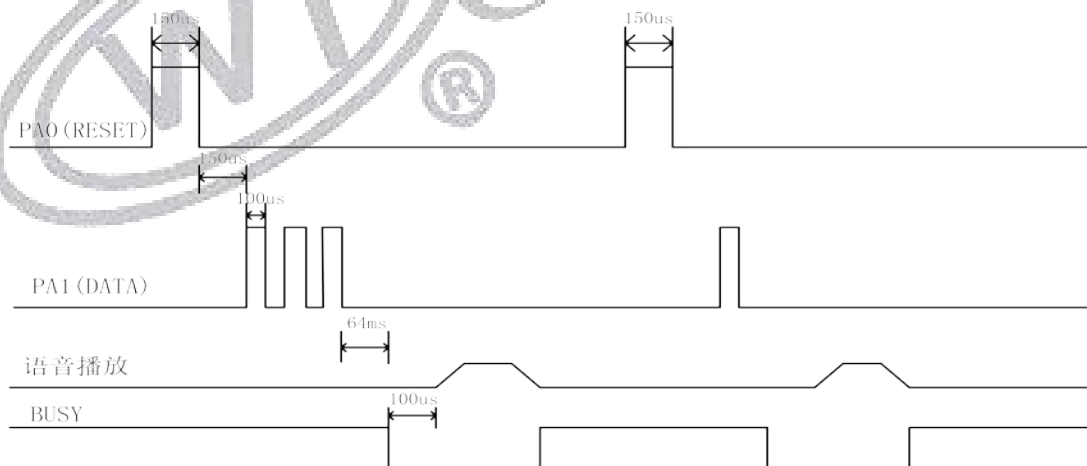
8.1. Pin Assignment:

Package	pin		
	PA2	PA1	PA0
SOP8	The default is BUSY signal output terminal	DATA	RESET

8.2. Voice Address Correspondence

No.	Number of pulses	Voice address
1	1	1
2	2	2
3	3	3
.....
222	222	222
223	223	223

8.3. Timing of Pulse Control



In the count pulse control sequence, first pull up the RESET signal by 150µs, and then send DATA. The high level of the pulse in DATA needs to be maintained at a high level of 100µs, and the interval between two pulses needs to be 100µs. 64ms after the pulse data is sent, the BUSY signal is output. After BUSY output 100µs, it will start to play the address voice, and the BUSY will also change after the voice playback.

Note: The pulse signal high-level width time range: 50µs~2ms, 100µs is recommended; the pulse signal

interval time range: 100us~4ms, 100us is recommended. The high level range of the reset signal is greater than 100us, and 150us is recommended. The communication IO port is usually low, and it should be pulled low after sending the data.

9. Button Control Mode:

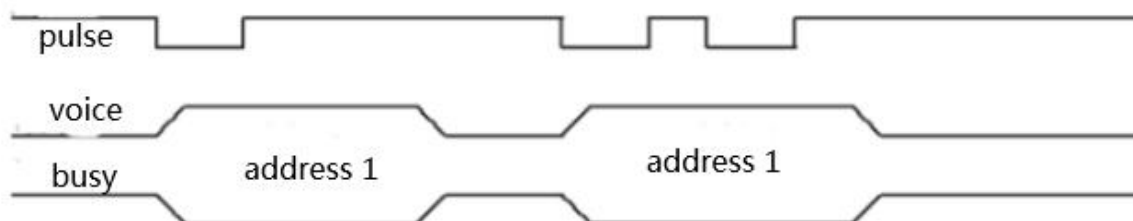
The defined pins can directly trigger the chip to play, that is, each pin can control the playback of a voice. The trigger mode of each pin can be set separately. The anti-shake time of the key control mode is 10ms. The key trigger module includes pulse repeatable trigger, pulse non-repeat trigger, level hold cycle, level hold non-cycle, next cycle, previous cycle. Please see the timing diagram below for details:

9.1. Pulse can be triggered repeatedly



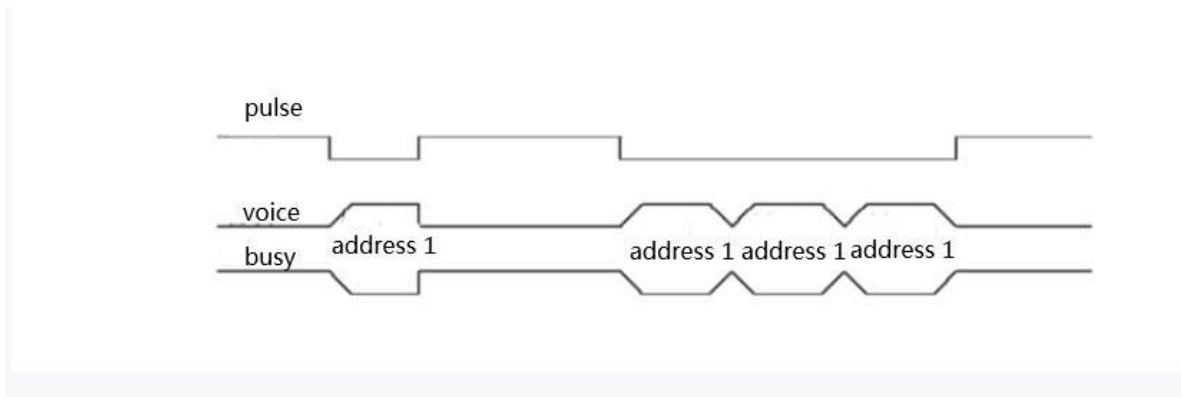
Note: Negative pulse trigger. When the I/O port detects a falling edge (for example, the I/O port is short-circuited to ground), the voice will be played. During the voice playback, when the falling edge is detected again, the chip will interrupt the voice being played and replay it. As long as there is a falling edge signal, it will replay.

9.2. Pulse can not be triggered repeatedly



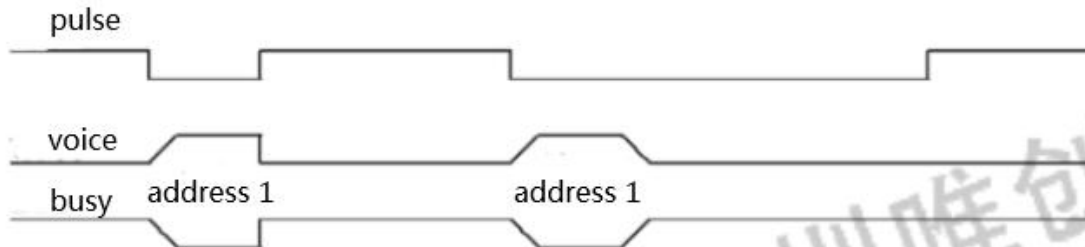
Note: Negative pulse trigger. When the I/O port detects a falling edge (for example, the I/O port is short-circuited to ground), the voice will be played. During the voice playback, when the falling edge is detected again, the chip does not act. The detected falling edge is not valid until the end of the voice.

9.3. Level Hold Loop



Remarks: When the I/O port is low level, keep playing, and stop when high level. When the first pass is over and the low level is still maintained, the playback will continue until it changes to the high level. As long as it is low level, there is sound; high level, there is no sound.

9.4. Keep the level without looping



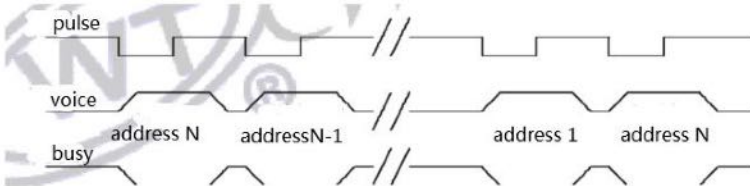
Remarks: Low level trigger. When the I/O port is low level, keep playing, and stop when high level. When the first play is over, the low level is still maintained, and the play will not continue. After the trigger, the play will end only once. If you need to replay, you need to keep the I/O port at a high level, then pull it to a low level, and then keep it at a low level.

9.5. The next song can be looped



Note: Negative pulse trigger. Use a button to trigger the playback of the voice. A negative pulse triggers the playback of a segment of voice, the next pulse triggers the playback of the next segment of voice, repeat the operation, after the last segment of voice is played, the first segment of voice will be on-demand, and this loop triggers the playback of voice.

9.6. The previous song can be looped



Note: Negative pulse trigger. Use a button to trigger the playback of the voice. A negative pulse triggers the playback of a segment of voice, the next pulse triggers the playback of the previous segment of voice, repeat the operation, after playing the most previous segment of voice, it will be ordered to the last segment of voice, and this loop triggers the playback of voice.

10. Program Example

10.1. One-line serial port control program

```

#define UC8 unsigned char
#define P_DATA P01
/*-----
;Module name:Line_1A_WTN6(UC8 DDATA)
;feature: achieve one-line serial communication functions
;Input parameters: DDATA is sending data
;output parameters
;P_DATA is the data port
;-----*/
Void Line_1A_WTN6( UC8 DDATA)
{
    UC8 S_DATA, j;
    bit B_DATA;

    S_DATA = DDATA;
    P_DATA = 0;
    Delay_1ms(5); //delay 5ms
    B_DATA = S_DATA&0X01;

    for(j=0; j<8; j++)
    {
        if(B_DATA == 1)
        {
            P_DATA = 1;
            Delay_N10us(60); //delay 600us
            P_DATA = 0;
            Delay_N10us(20); //delay 200us
        }
        else
        {
            P_DATA = 1;
            Delay_N10us(20); //delay 200us
            P_DATA = 0;
            Delay_N10us(60); //delay 600us
        }
        S_DATA = S_DATA>>1;
        B_DATA = S_DATA&0X01;
    }
}

```



```
P_DATA = 1;
}
```

10.2. Two-line serial port control program

```
#define UC8    unsigned char
#define CLK_2A    P01
#define P_DATA_2A P00

/*-----
;Module name:Line_2A_WTN6(UC8 DDATA)
;Function: Realize two-line serial communication function
;Input parameters: DDATA is sending data
;Output parameters
; CLK_2A //Clock line
; P_DATA_2A //data line
;-----*/
Void Line_2A_WTN6(UC8 DDATA)
{
    UC8 S_DATA,j;
    bit B_DATA;
    CLK_2A = 1; //Clock line
    P_DATA_2A = 1; //data line

    S_DATA = DDATA;
    CLK_2A = 0;
    Delay_1ms(5); //delay 5ms
    B_DATA = S_DATA&0X01;
    for(j=0;j<8;j++)
    {
        CLK_2A = 0; // Pull down
        P_DATA_2A = B_DATA; //Transmission data one bit

        Delay_N10us(30); //delay 300us
        CLK_2A = 1; //Pull up
        Delay_N10us(30); //delay 300us

        S_DATA = S_DATA>>1;
        B_DATA = S_DATA&0X01;
    }
    P_DATA_2A = 1;
    CLK_2A = 1;
}
```

10.3. Count Pulse Control Program

```

#define UC8          unsigned char
#define RST          P00
#define DATA_CLK   P01
/*-----
;Module name:Line_one
;Function: send the number of pulses of the specified address
;Input parameters: DDATA is the number of pulses
;Output parameters:0
;RST is the reset signal
;DATA_CLK is a pulse signal
;-----*/
void Line_one(UC8  DDATA)
{
    UC8  i;
    RST   = 0;
    DATA_CLK = 0;

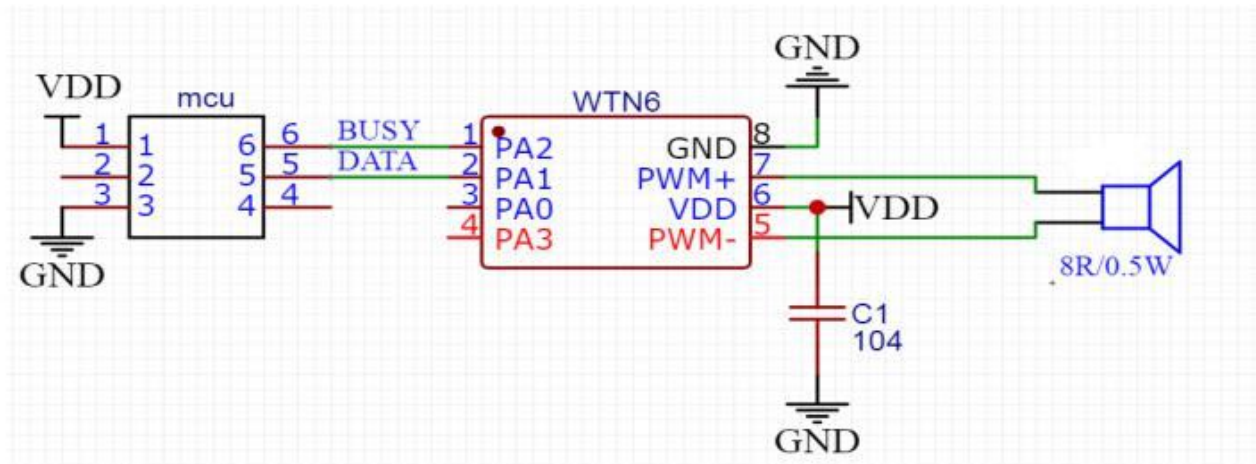
    RST   = 1;           // Pull high reset
    Delay_N10us(15);    //delay
    RST   = 0;           // Pull down
    Delay_N10us(15);
    for(i=0;i<DDATA;i++)
    {
        DATA_CLK = 1;
        Delay_N10us(10);
        DATA_CLK = 0;
        Delay_N10us(10);
    }
    RST   = 0;
    DATA_CLK = 0;
}

```

11. Application Circuit

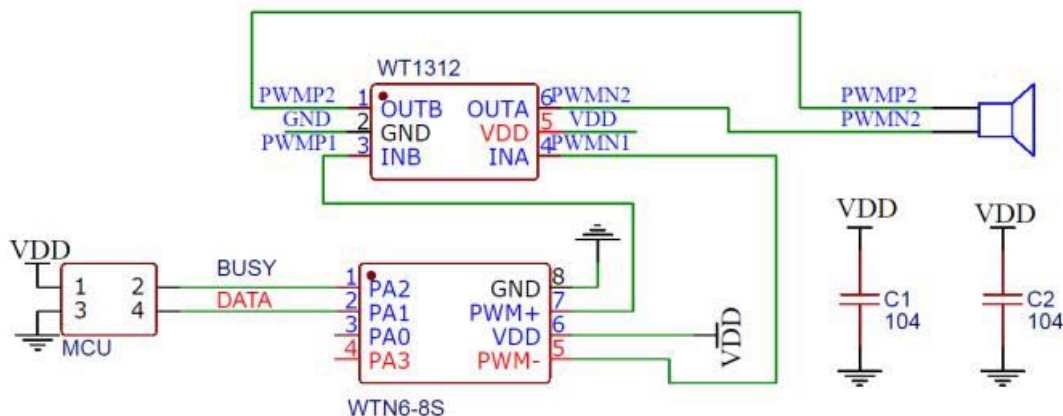
11.1. One-line Serial Port

The working voltage range of the voice chip is 2.4V-5.2V, PWM output



Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips.

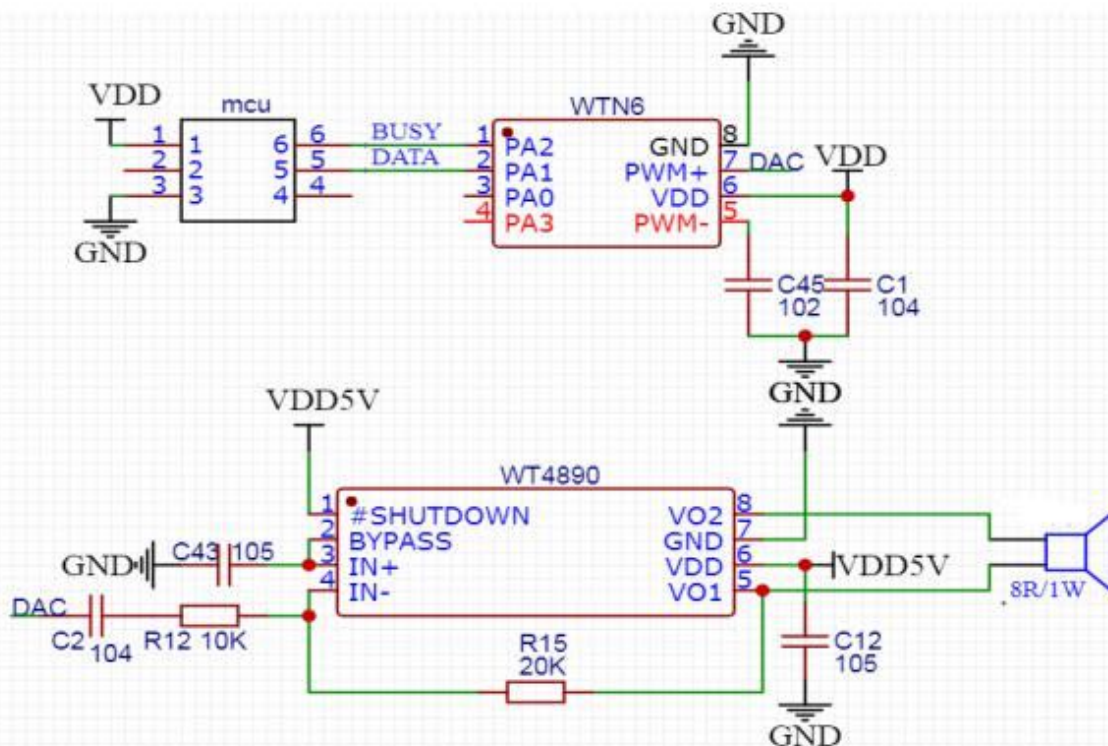
The working voltage range of the voice chip is 2.4V-5.2V, the working voltage range of the power amplifier chip is 1.8V-6.0V, and the output of the external PWM power amplifier



Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips.

The WT1312 power amplifier is a PWM power amplifier and can only be used in PWM output mode.

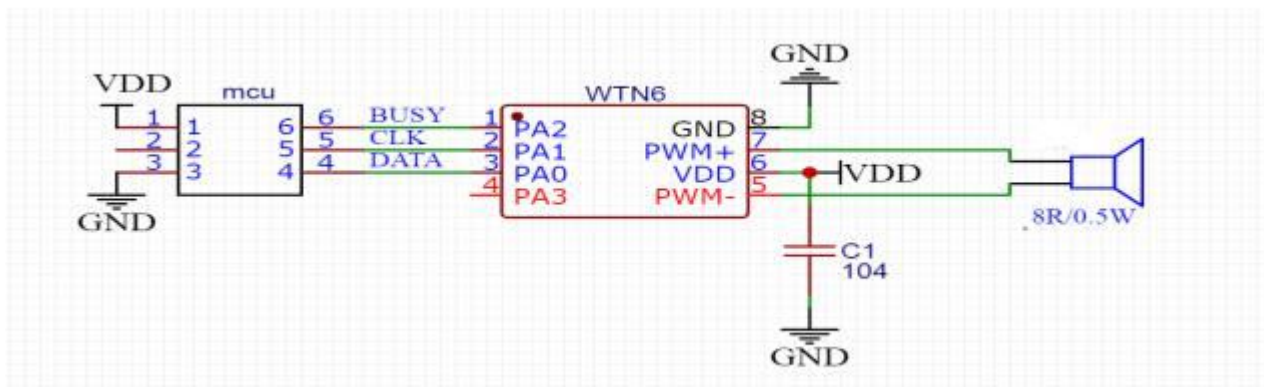
The working voltage range of the voice chip is 2.4V-5.2V, DAC output



Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips. In the DAC output mode, the PWM-pin must be connected to a 1nf capacitor to the ground, and the DAC output can be connected to an external power amplifier to drive a louder speaker.

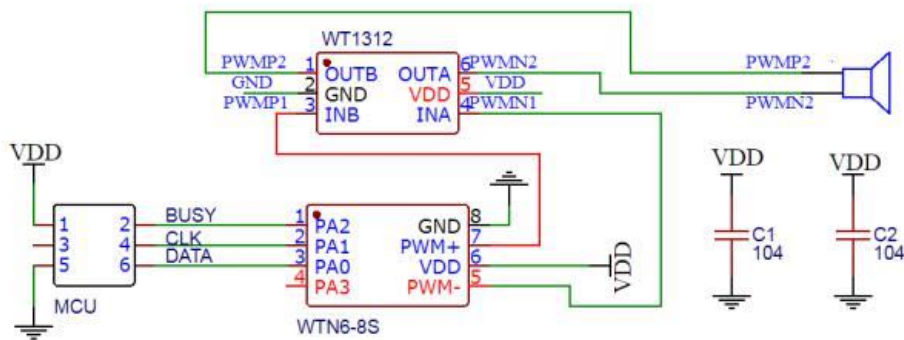
11.2. Two-line Serial Port

The working voltage range of the voice chip is 2.4V-5.2V, PWM output:



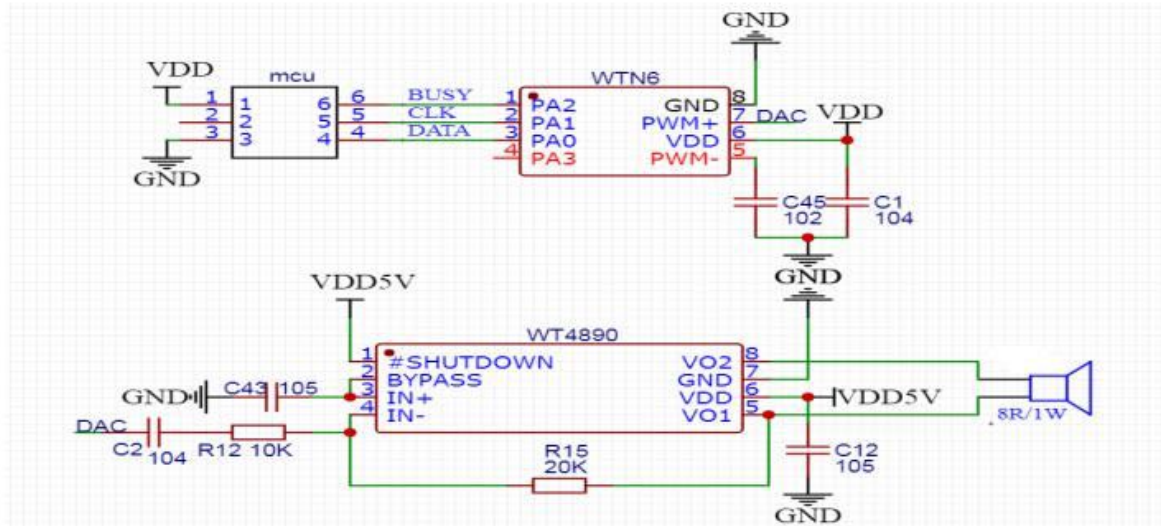
Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips.

The working voltage range of the voice chip is 2.4V-5.2V, the working voltage range of the power amplifier chip is 1.8V-6.0V, and the output of the external PWM power amplifier



Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips.

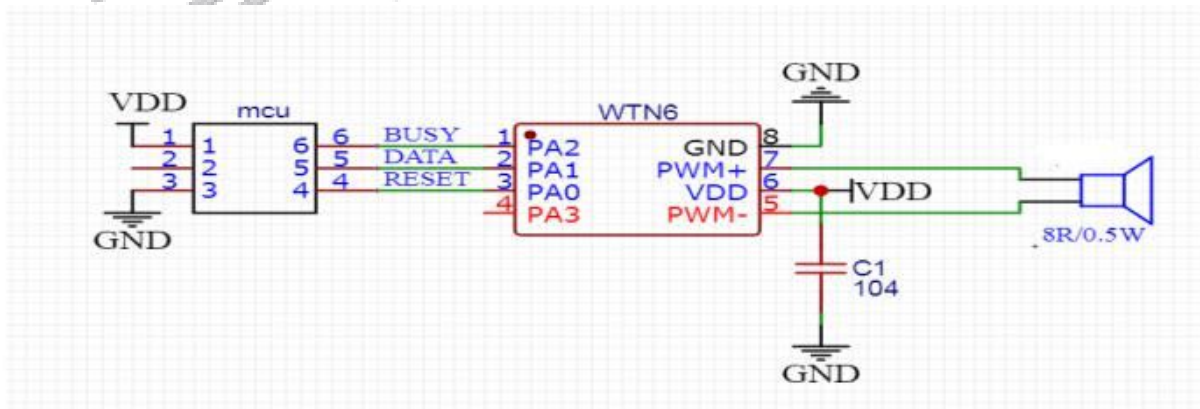
The WT1312 power amplifier is a PWM power amplifier and can only be used in PWM output mode.



Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips. In the DAC output mode, the PWM-pin must be connected to a 1nf capacitor to the ground, and the DAC output can be connected to an external power amplifier to drive a louder speaker.

11.3. Count pulse application circuit:

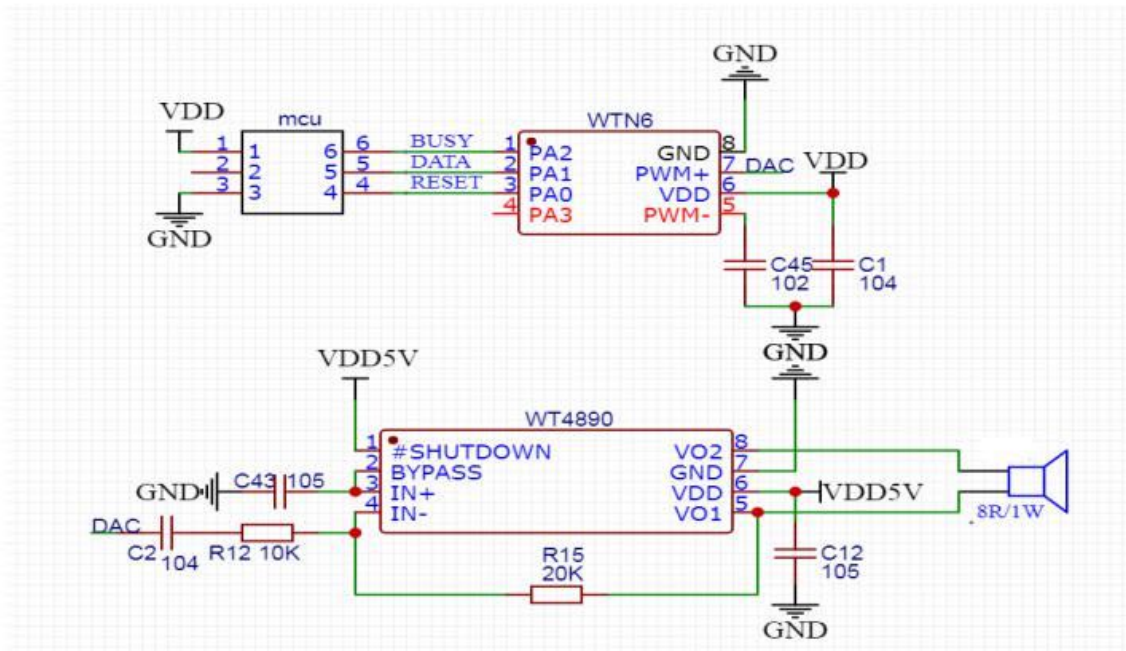
The working voltage range of the voice chip is 2.4V-5.2V, PWM output



Note:

When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips.

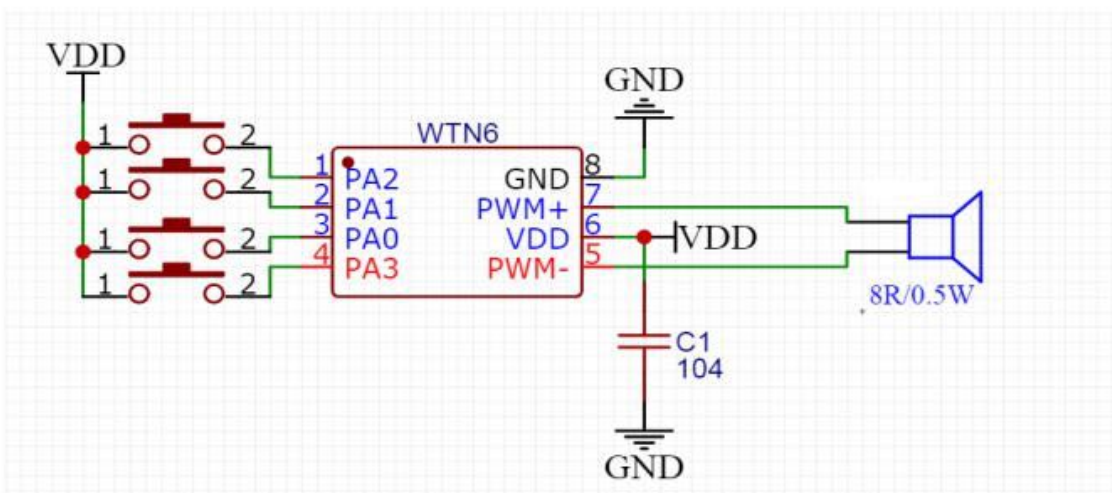
The working voltage range of the voice chip is 2.4V-5.2V, DAC output



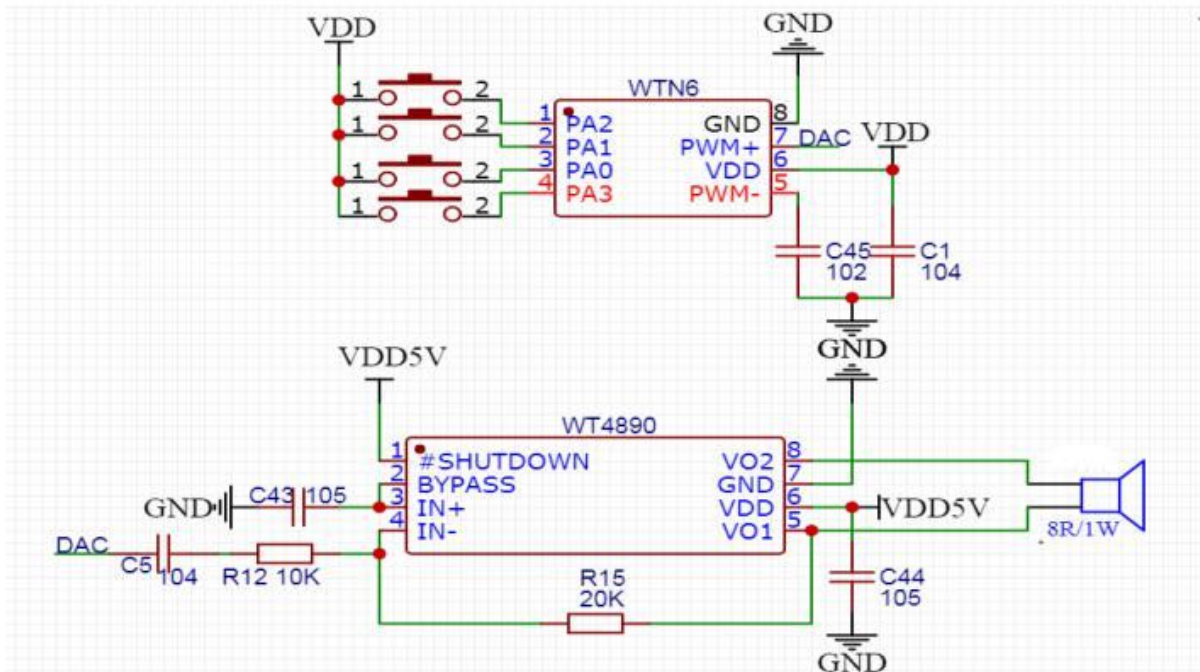
Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips. In the DAC output mode, the PWM-pin must be connected to a 1nf capacitor to the ground, and the DAC output can be connected to an external power amplifier to drive a louder speaker.

11.4. Button Application Circuit (high level trigger control)

The working voltage range of the voice chip is 2.4V-5.2V, PWM output



Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips.



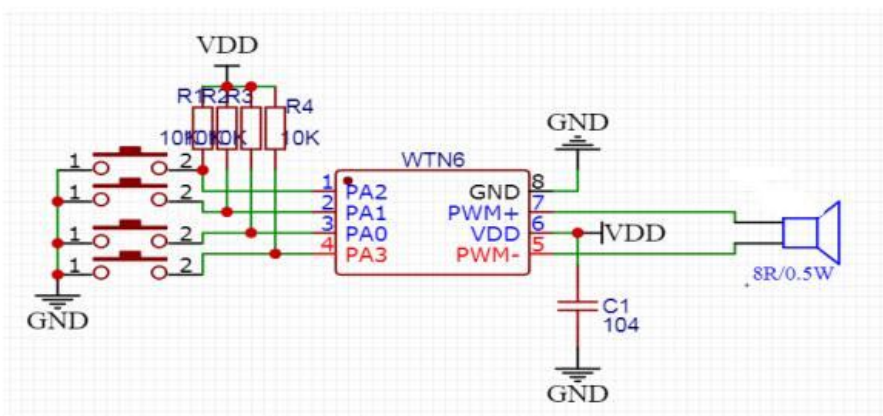
The

working voltage range of the voice chip is 2.4V-5.2V, DAC output

Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips. In the DAC output mode, the PWM-pin must be connected to a 1nf capacitor to the ground, and the DAC output can be connected to an external power amplifier to drive a louder speaker.

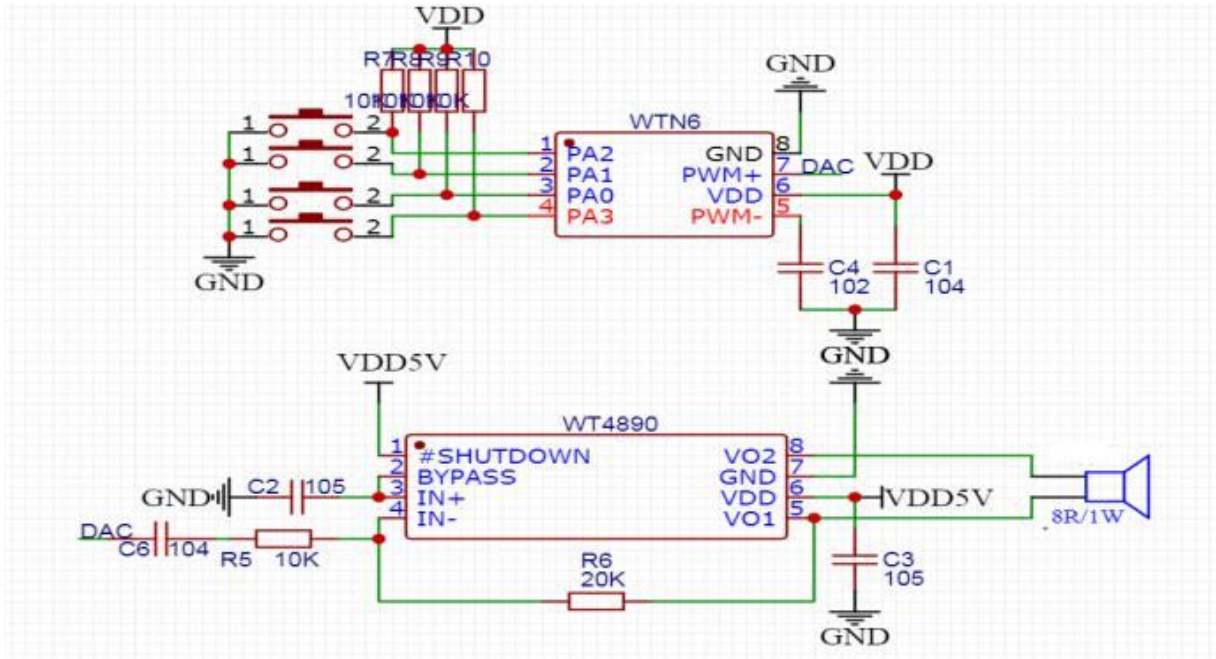
11.5. Button Application Circuit (Low Level Trigger Control)

The working voltage range of the voice chip is 2.4V-5.2V, PWM output

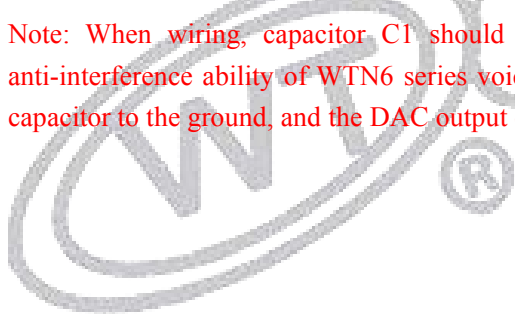


Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips.

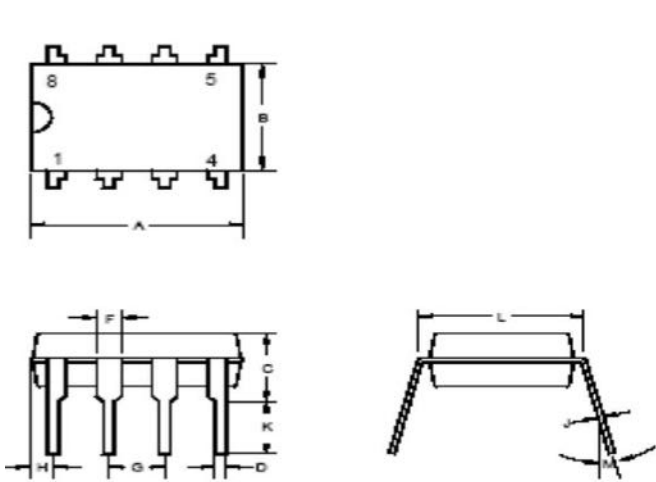
The working voltage range of the voice chip is 2.4V-5.2V, DAC output



Note: When wiring, capacitor C1 should be as close as possible to the VDD pin of WTN6 chip to enhance the anti-interference ability of WTN6 series voice chips. In the DAC output mode, the PWM-pin must be connected to a 1nf capacitor to the ground, and the DAC output can be connected to an external power amplifier to drive a louder speaker.

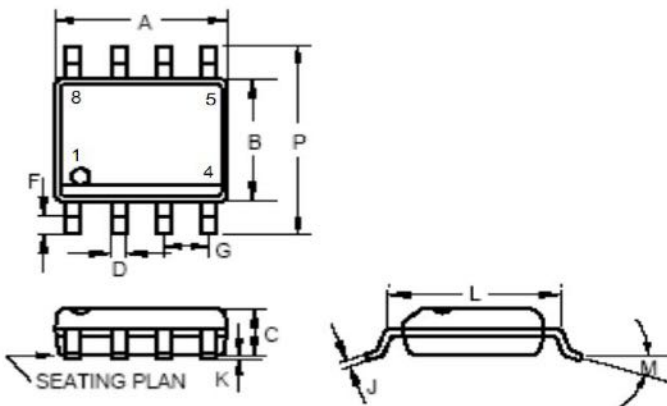


12. Package Pin Diagram



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.355	0.365	0.400	9.02	9.27	10.16
B	0.240	0.250	0.280	6.10	6.35	7.11
C	-	-	0.210	-	-	5.33
D	-	0.018	-	-	0.46	-
F	-	0.060	-	-	1.52	-
G	-	0.100	-	-	2.54	-
H	0.050	-	0.090	1.27	-	2.29
J	0.008	-	0.015	0.20	-	0.38
K	0.115	0.130	0.150	2.92	3.30	3.81
L	0.300 BSC.			7.62 BSC.		
M	-	7°	15°	-	7°	15°

Waytronic



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.183	-	0.202	4.65	-	5.13
B	0.144	-	0.163	3.66	-	4.14
C	0.068	-	0.074	1.35	-	1.88
D	0.010	-	0.020	0.25	-	0.51
F	0.015	-	0.035	0.38	-	0.89
G	0.050 BSC			1.27 BSC		
J	0.007	-	0.010	0.19	-	0.25
K	0.005	-	0.010	0.13	-	0.25
L	0.189	-	0.205	4.80	-	5.21
M	-	-	8°	-	-	8°
P	0.228	-	0.244	5.79	-	6.20

Note: For 8-pin S.O.I.C., 100 units per tube.